PVP 14

Code: EC5T5

III B.Tech - I Semester–Regular Examinations December 2016

DIGITAL IC APPLICATIONS
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Define and list Variable data types.
b) Write the differences between Reg and Wire data types in verilog HDL.
c) List four kinds of loop statements in verilog.
d) Define logic family and what are the different kinds of logic families?
e) Show the logic levels and noise margins for the HC-series CMOS logic family.
f) Draw full subtractor logic symbol and its functions.
g) Difference between latches and flip-flops.
h) Draw the block diagram of Mealy-machine.
i) What are the applications of counters?
j) Draw the circuit diagram for a T-FF using JK - FF.
k) What is the function of decoder in memory? What is the size of the decoder required for the 1024x8 bit size ROM?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) What are the different categories of operators in Verilog HDL? Explain any four with examples. 8 M

   b) Explain built-in-primitive gates in gate-level modeling of verilog HDL. 8 M

3. a) Explain characteristics of TTL families. 8 M

   b) Compare CMOS, TTL and ECL logic families with respect to propagation delay and noise margin. 8 M

4. a) Explain and draw 74x280, 9-bit odd/even parity generator and applications of parity-checking. 8 M

   b) Construct 8-to-3 binary encoder and write the verilog code for the same. 8 M

5. a) Explain the functional behavior of positive edge triggered D-FF. 8 M

   b) Explain structure of serial in parallel out shift register 74x164, 8-bit logic symbol. 8 M

6. a) Draw and explain the internal ROM structure showing the use of control inputs. 8 M

b) Explain various commercial ROM types available. 8 M